IN THE SPECIFICATION

Please amend the paragraph at page 22, line 11 to page 23, line 9, as follows:

Next, a resist pattern 17a having an ordinary thickness for forming the source line 5, the source terminal portion metal pad 5a and the drain electrode 7 and a thin film resist pattern 17b for forming the semiconductor active layer 8 of the thin film transistor are provided at a second photolithographic step as shown in Fig. 4. A novolak resin based positive resist is used and the resist is coated in a thickness of 1.5 μm by a spin coater. After the resist is coated, prebaking is carried out for 90 seconds at a temperature of 120° C. Then, exposure is carried out for 1000 milliseconds by using a mask pattern including the resist pattern 17a and the resist pattern 17b. Thereafter, additional exposure ~~sis~~ is carried out for 400 milliseconds by using a mask pattern capable of exposing only the resist pattern 17b in a semiconductor active layer portion. By carrying out the exposure in two stages, the resist pattern 17a having an ordinary thickness and the thin film resist pattern 17b have different thicknesses. An exposing machine is of a stepper or mirror projection type, and g rays and h rays of a high pressure mercury are used for a light source. Subsequently, development is carried out by using an organic alkali based developing solution and postbaking is then carried out for 180 seconds at a temperature of 100° C to 120° C. Consequently, a solvent in the resist is volatilized and the adhesion of the resist and Cr is increased. By these processes, the resist of the thin film transistor portion has a shape shown in Fig. 10. A thickness of the resist film of the resist pattern 17a having an ordinary thickness is approximately 1.4 μm and a thickness of the resist of the thin film resist pattern 17b is approximately 0.4 μm.

Please amend the paragraph at page 25, line 16 to page 26, line 3, as follows:

Fig. 2(a) is a sectional view of a TFT portion, Fig. 2(b) is a sectional view of a gate terminal portion, Figs. 2(c) and 2(d) are sectional views of each source terminal portion. The

source terminal may be formed of source line layer 5a as shown in Fig. 2(c). Alternatively, the source terminal may be formed of the material of the gate line 1, into which source line layer 5a is converted at an intervening part of source terminal as shown in Fig. 2(d). The intervening part where the source line layer 5a is converted into the gate line 1 is situated under a repair line for the source line, where the repair line is formed of a material of the source line, or in the vicinity of a seal portion or liquid crystal portion. By virtue of converting the material of the source line into the material of the gate line, the source line can be prevented from being corroded in the vicinity of the ~~sourere~~ source terminal portion, so that disconnection of the source line can be avoided.

Please amend the abstract at page 98, lines 2-8, as follows:

~~The present invention is a~~ A thin film transistor array substrate ~~includes:~~ including an insulating substrate[[;]], a first metallic pattern formed on ~~said~~ ~~insulting~~ the insulating substrate[[;]], and an insulating film provided on ~~said~~ the first metallic pattern~~; a~~. A semiconductor pattern is provided on ~~said~~ the insulating film[[;]], and a second metallic pattern is provided on ~~said~~ the semiconductor pattern~~; wherein said~~. The second metallic pattern is surrounded by ~~said~~ the semiconductor pattern.